ABSTRACT

This paper describes a single-chip media processor for use in Digital Television (DTV) applications and covers its features, system interfaces and application areas.

INTRODUCTION

This single DTV media processor chip (DTV-processor) is targeted for digital television-related markets using the ATSC digital standard. DTV-processors can be designed into high or standard definition digital television systems, as well as digital set-top boxes, etc. There are six key functions in ATSC standard based digital television applications:

- Transport stream demux
- MPEG2 MP@HL video decoding
- AC-3 audio decoding
- Clock recovery from the bitstream; video-audio synchronization and bitstream buffer management
- Graphics for closed caption, user interface and program guide, etc.
- Display video format conversion, which includes horizontal and vertical scaling, interlaced to non-interlaced or non-interlaced to interlaced conversions and blending of graphics surfaces with the video surface.

A combination of hardware and software implements the above key functions in the DTV-processor.

DTV-PROCESSOR OVERVIEW

The DTV-processor consists of a Very Long Instruction Word (VLIW) CPU core, large instruction and data caches, input/output units, media co-processor units, and high performance busses and memory system. The VLIW processor core (the DSPCPU) coordinates all on-chip activities. In addition to implementing the non-trivial parts of multimedia algorithms, this processor runs a small real-time operating system that is driven by interrupts from the other units. The DMA-driven input/output units operate independently, and correctly format the data to make software media processing efficient. The DMA-driven multimedia coprocessor units operate independently and in parallel with the DSPCPU to perform operations specific to important multimedia algorithms. The high-performance busses and memory system communicate between processing units within the DTV-processor.

At the heart of the DTV-processor chip is the powerful 32-bit DSPCPU core. This implements a 32-bit linear address space and 128 fully general-purpose 32-bit registers. The core uses a VLIW instruction-set architecture and is itself fully general-purpose. With 27 functional units, the DTV-processor can issue five operations every cycle. The functional units include integer and floating-point arithmetic units and a data-parallel DSP-like unit.

Using a VLIW architecture maximizes processor throughput at the lowest possible cost. The DSPCPU core is supported by separate 32 kB instruction and 16 kB data caches. This data cache is dual-ported, and both caches are eight-way set-associative with a 64-byte block size.

Figure 1 shows a system block diagram of the DTV-processor chip, with the main memory interface using the 64-bit wide data bus. The glueless PCI interface directly connects the DTV-processor to many PC-based peripheral chips. The time-multiplexed XIO bus allows general purpose chips such as ROM to be connected gluelessly to the DTV-processor. A high-definition video out (video out HD) interface can be connected to a standard or high-definition TV monitor through a set of D/A converters.

Two audio-in interface units allow the capture of two different sources of PCM data for stereo audio input or SPDIF data through external glue logic. Both audio input ports support 16-bit data per channel.

There are two audio-out units, with each unit capable of operating at an independent sample rate. One unit outputs 6-channel PCM data for AC-3 audio and 2-channel PCM data for stereo audio, and the other unit outputs 2-channel PCM data for stereo audio. All audio-out channels support a maximum of 32 bits per channel.

Finally, the V.34/ISDN interface requires only an external front-end chip and phone line interface to provide remote communication support.

1. The IC is available commercially as PTM2700.
DTV-PROCESSOR IN DIGITAL TV SYSTEMS

The system block diagram (Figure 1) shows the new DTV media processor with its video, audio, communication and control interfaces. The major functions of the digital television are described below.

Transport Stream Capture and PID filtering

The transport input unit receives the transport stream data and performs the PID filtering to select the required transport packets.

Transport Demux

Separating the video and audio elementary streams is called transport stream demuxing. The demux operation is completely performed by the DSPCPU, in software.

Video Decoder

The MPEG2 MP@HL video decoding is performed by the DSPCPU and the MPEG-PIPE hardware.

Display Process

The DSPCPU instructs the on-chip high-definition video-out unit (HDVO) to render a given field or frame from the main memory to the external TV monitor through a set of DACs. The HDVO can output the pixels in several formats including RGB888. The DSPCPU includes an option to instruct the HDVO unit to scale the given image horizontally and vertically.

Graphics

Graphics required for digital television applications are implemented in the DSPCPU and the HDVO unit. The graphics application includes electronic program guide and user interfaces.

Audio Decode and Audio Output

The ATSC digital television standard makes use of the AC-3 audio stream. The audio bitstream is completely decoded in software, and the output audio data is stored in the main memory. The audio-out DMA unit reads the decoded audio PCM data and drives the external audio DACs.

System Control

There is a concurrent system control task which runs under the pSos operating system kernel to manage all the tasks related to the digital television application. The peripheral units use interrupt mechanisms to communicate their status to the system control task.

APPLICATIONS

The DTV-processor can be used in digital televisions, set-top boxes, and PC-TV applications. It will also make new applications possible such as discretionary content processing, video conferencing, web browsing and 3D game playing.

When the DTV-processor is provided with a standard-definition video signal, it can perform film/video detection and intelligent motion-estimation-based image improvement. This enables it to show an enhanced quality image on the high-definition display device.

CONCLUSION

A highly integrated DTV-processor chip uses the ATSC transport stream as input and provides the audio, video and graphics as output. The DTV-processor is the world’s first IC to perform most of the DTV receiver functions in one chip.

Fig.1 Typical DTV media processor-based system.